National Workshop
on
VLSI DESIGN FLOW USING CADENCE EDA TOOL
(NWOCT-2016)

cadence

25th May 2016 - 26th May 2016

In Association with

Entuple Technologies Pvt .Ltd.
Indian Society for Technical Education
(SKIT Student Chapter)
The Institution of Electronics and Telecommunication Engineers
(SKIT Student Chapter)

Organized by
Department of Electronics & Communication Engineering
(NBA Accredited-B.Tech Programme)

Co-Convener	**Convener**	**Secretary**
Mr. Vikas Pathak	Prof. (Dr.) S. K. Bhatnagar	Ms. Mamta Jain
Ms. Pooja Choudhary	HOD ECE	Ms. Manju Choudhary

Important Dates

Registration Deadline **May, 21, 2016**
Intimation of Confirmation **May, 23, 2016**
Email: vlsidesigncadence@gmail.com
Limited seats, apply in advance

Registration form is to be filled online through the link given below
http://goo.gl/forms/FO2VuFp9C4

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